33.6.1.2.8 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.6 and 33.2.7. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting Delivering Power. The combinations '101', '110' and '111' for bits 12.6:4 have been reserved for future use.

33.6.1.2.9 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as '000', bits 12.3:1 indicate that the PSE state diagram (Figure 33–6) is in the state DISABLED. When read as '010', bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as '100', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as '101', bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as '001', bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations '111' and '110' for bits 12.3:1 have been reserved for future use.

33.6.1.2.10 Pair Control Ability (12.0)

When read as a logic one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a logic zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.7 Protocol Implementation Conformance Statement (PICS) proforma for Clause 33, DTE Power via MDI

33.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3af-2003, DTE Power via MDI, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.7.2 Identification

33.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	

1—Required for all implementations

2—May be completed as appropriate in meeting the requirements for the identification.

3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).

33.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3af-2003, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

33.7.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDCL	PD Classification	33.3.4	PD supports classification	O	Yes [ ] No [ ]

33.7.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CL	Implementation supports classification	33.2.7	Optional	O	Yes [ ] No [ ]
*END	Endpoint PSE	33.2.1	PSE implemented as an end-point device	O/1	Yes [ ] No [ ]
*ENDA	Alternative A Endpoint PSE	33.2.1	PSE implements Alternative A	END:O.2	Yes [ ] No [ ]
*ENDB	Alternative B Endpoint PSE	33.2.1	PSE implements Alternative B	END:O.2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.6	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a mid-span device	O/1	Yes [ ] No [ ]
*PA	Power Allocation	33.2.9	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability - PSE supports the option to control which PSE Pinout is used	33.6.1.1.3	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.10.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.10.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

33.7.3 PICS proforma tables for DTE Power via MDI

33.7.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility Considerations.	33.1.2	PDs and PSEs compatible at their PIs.	M	Yes [ ]

33.7.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location.	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated.	M	Yes [ ]
PSE2	Alternative B.	33.2.1	Only implementation allowed for Midspan.	MID:M	Yes [ ] N/A [ ]
PSE3	Alternative A and Alternative B.	33.2.2	Not operate on same link segment simultaneously.	END:M	Yes [ ] N/A [ ]
PSE4	PSE behavior.	33.2.3	In accordance with state diagrams shown in Figure 33–6 and Figure 33–7.	M	Yes [ ]
PSE5	Detection, classification and turn on timing.	33.2.3.1	In accordance with Table 33–5.	M	Yes [ ]
PSE6	Turn on power.	33.2.3.1	After valid detection in less than Tpon.	M	Yes [ ]
PSE7	Not apply power within Tpon.	33.2.3.1	Must initiate and successfully complete a new detection cycle before applying power.	M	Yes [ ]
PSE8	Alternative B backoff cycle.	33.2.3.1	Must wait no less than T_{dbo} as specified in Table 33–5 before attempting another detection.	M	Yes [ ]
PSE9	Backoff voltage.	33.2.3.1	Not greater than 2.8Vdc.	M	Yes [ ]
PSE10	Applying power.	33.2.4	Not until a PD requesting power has been successfully detected.	M	Yes [ ]
PSE11	Power pairs.	33.2.4	Power must be supplied on the same pairs as those used for detection.	M	Yes [ ]
PSE12	Detecting PDs.	33.2.5	Performed via the PSE PI.	M	Yes [ ]
PSE13	Open circuit voltage.	33.2.5	Item 1 in Table 33–2.	M	Yes [ ]
PSE14	Short circuit current.	33.2.5	Item 2 in Table 33–2.	M	Yes [ ]
PSE15	Backdriven current.	33.2.5	Not be damaged by up to 5mA over the range of Vport.	M	Yes [ ]
PSE16	Output capacitance.	33.2.5	Item 18 in Table 33–5.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE17	Exhibit Thevenin equivalence to one of the detection circuits in all detection states.	33.2.5	Figure 33–8 or Figure 33–9.	M	Yes [ ]
PSE18	V_{detect} with a valid PD signature connected.	33.2.5.1	Item 3 in Table 33–2.	M	Yes [ ]
PSE19	Two measurements with V_{detect}.	33.2.5.1	At least 1 V difference between consecutive measurements.	M	Yes [ ]
PSE20	Control slew rate when switching detection voltages.	33.2.5.1	Item 6 in Table 33–2.	M	Yes [ ]
PSE21	Polarity of $V_{detect.}$	33.2.5.1	Match polarity of V_{Port} defined in 33.2.1.	M	Yes [ ]
PSE22	Probe link to detect all PDs which present a valid signature.	33.2.6.1	(19KΩ to 26.5KΩ DC resistance) and (120nF capacitance or less) and (Voltage offset of up to 2.0 volts DC) and (Current offset of up to 12μA).	M	Yes [ ]
PSE23	Reject PDs that present an invalid signature.	33.2.6.2	(Less than 15 KΩ DC resistance) or (More than 33 KΩ DC resistance) or (More than 10μF capacitive load).	M	Yes [ ]
PSE24	Default classification.	33.2.7	Assign to Class 0 if PD cannot be classified as Class 1, 2, 3, or 4.	M	Yes [ ]
PSE25	Classification power levels	33.2.7.1	PDs classified as Class 4 will be treated as Class 0.	M	Yes [ ]
PSE26	Provide $V_{Class.}$	33.2.7.2	Between 15.5 and 20.5 volts, limited to 100 mA or less at the PI.	CL:M	Yes [ ] N/A [ ]
PSE27	Classification polarity	33.2.7.2	Same as V_{Port}.	CL:M	Yes [ ] N/A [ ]
PSE28	Classification timing	33.2.7.2	Item 20 in Table 33–5.	CL:M	Yes [ ] N/A [ ]
PSE29	Measure $I_{Class.}$	33.2.7.2	Classify PD according to Table 33–4.	CL:M	Yes [ ] N/A [ ]
PSE30	Classification default.	33.2.7.2	Assign PD to Class 0 if I_{class} is greater than or equal to 51mA.	CL:M	Yes [ ] N/A [ ]
PSE31	Power supply output.	33.2.8	Provide power to the PI according to Table 33–5, Figure 33–6, and Figure 33–7.	M	Yes [ ]
PSE32	Output Voltage	33.2.8.1	The specification for V_{Port} includes line and temperature variations.	M	Yes [ ]
PSE33	V_{Port} measurement.	33.2.8.1	Measured between any conductor of one power pair and any conductor of the other power pair.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE34	Load regulation.	33.2.8.2	Specified as 0.44W to 15.4W load step at a rate of change of 35mA/μs max.	M	Yes [ ]
PSE35	Voltage transients	33.2.8.2	Limited to 3.5V/μs max.	M	Yes [ ]
PSE36	Power feeding ripple and noise	33.2.8.3	Met for common-mode and/or pair-to-pair noise values for power outputs from 0.44W to 15.4W at operating V_{Port}.	M	Yes [ ]
PSE37	Maximum current at minimum voltage	33.2.8.4	For $V_{Port} > 44V$, the minimum value for I_{Port_max} in Table 33–5 shall be $15.4W/V_{Port}$	M	Yes [ ]
PSE38	AC current waveform parameters	33.2.8.4	I_{Peak} = 0.4A minimum for 50ms minimum and 5% duty cycle minimum. For $V_{Port} > 44V$, $I_{Peak} = 17.6W/V_{Port}$.	M	Yes [ ]
PSE39	Specifications for I_{Inrush} current	33.2.8.5	Meet conditions specified in 33.2.8.5 items a) through e).	M	Yes [ ]
PSE40	Overload current detection range	33.2.8.6	If $I_{port} > I_{CUT}$ for $T > T_{ovld}$ the PSE shall remove power. Item 8 in Table 33–5	M	Yes [ ]
PSE41	Overload time limit.	33.2.8.7	Item 9 in Table 33–5	M	Yes [ ]
PSE42	Short circuit current	33.2.8.8	Item 10 in Table 33–5.	M	Yes [ ]
PSE43	Short circuit time limit	33.2.8.9	Item 11 in Table 33–5.	M	Yes [ ]
PSE44	Turn off time	33.2.8.10	Applies to the discharge time from V_{Port} to 2.8Vdc with a test resistor of 320KΩ attached to the PI.	M	Yes [ ]
PSE45	Turn off voltage	33.2.8.11	Applies to the PI voltage in the IDLE State.	M	Yes [ ]
PSE46	Current unbalance	33.2.8.12	Item 15 in Table 33–5.	M	Yes [ ]
PSE47	Power turn on time	33.2.8.13	Item 16 in Table 33–5.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE48	Power provision.	33.2.9	Do not initiate if PSE is unable to provide maximum power level requested by PD based on PD's classification.	PA:M	Yes [ ] N/A [ ]
PSE49	Power allocation.	33.2.9	Not be based solely on historical data of power consumption of the attached PD.	PA:M	Yes [ ] N/A [ ]
PSE50	PSE AC MPS component requirements.	33.2.10.1.1	Meet requirements specified in item 1 and item 3 in Table 33–6	AC:M	Yes [ ] N/A [ ]
PSE51	PSE AC MPS component present.	33.2.10.1.1	Meets requirements specified in item 4a in Table 33–6.	AC:M	Yes [ ] N/A [ ]
PSE52	PSE AC MPS component absent.	33.2.10.1.1	Meets requirements specified in item 4b in Table 33–6.	AC:M	Yes [ ] N/A [ ]
PSE53	Power removal.	33.2.10.1.1	When AC MPS has been absent for a time duration greater than T_{PMDO}.	AC:M	Yes [ ] N/A [ ]
PSE54	PSE DC MPS component present.	33.2.10.1.2	Meet requirements specified in item 6 and item 7b in Table 33–5.	DC:M	Yes [ ] N/A [ ]
PSE55	PSE DC MPS component absent.	33.2.10.1.2	Meet requirements specified in item 6 in Table 33–5.	DC:M	Yes [ ] N/A [ ]
PSE56	Power removal.	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{PMDO}.	DC:M	Yes [ ] N/A [ ]
PSE57	Not remove power.	33.2.10.1.2	When the DC current is greater than or equal to I_{Min2} max for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–5	DC:M	Yes [ ] N/A [ ]

33.7.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power.	33.3.1	On either set of PI conductors.	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–7.	M	Yes [ ]
PD3	Source power.	33.3.1	The PD will not source power on its PI.	M	Yes [ ]
PD4	Voltage tolerance.	33.3.1	Withstand 0V to 57V at the PI indefinitely without permanent damage.	M	Yes [ ]
PD5	PD behavior.	33.3.2	According to state diagram shown in Figure 33–13.	M	Yes [ ]
PD6	Valid detection signature.	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI.	M	Yes [ ]
PD7	Non-valid detection signature.	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI and will not accept power via the PI.	M	Yes [ ]
PD8	Non-valid detection signature.	33.3.3	When powered, present an invalid signature on the set of pairs not drawing power.	M	Yes [ ]
PD9	Valid detection signature.	33.3.3	Characteristics defined in Table 33–8.	M	Yes [ ]
PD10	Non-valid detection signature.	33.3.3	Exhibit one or both of the characteristics described in Table 33–9.	M	Yes [ ]
PD11	Return Class 0 to 3 classification.	33.3.4	Implement classification selection according to maximum power draw specified in Table 33–10.	PDCL:M	Yes [ ] N/A [ ]
PD12	Classification signature.	33.3.4	As defined in Table 33–11.	PDCL:M	Yes [ ] N/A [ ]
PD13	Classification signature.	33.3.4	One classification signature during classification.	PDCL:M	Yes [ ] N/A [ ]
PD14	PD power supply.	33.3.5	Operate within the characteristics in Table 33–12.	M	Yes [ ]
PD15	PD turn on voltage.	33.3.5.1	PD will turn on at a voltage less than V_{On}.	M	Yes [ ]
PD16	PD stay on voltage.	33.3.5.1	Must stay on for all voltages in the range of V_{Port}.	M	Yes [ ]
PD17	PD turn off voltage.	33.3.5.1	Must turn off at a voltage less than V_{Port} minimum and greater than V_{Off}.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD18	Input average power.	33.3.5.2	Applies for input power as specified in Table 33–12 averaged over one second.	M	Yes [ ]
PD19	Input inrush current.	33.3.5.3	Limited by the PD if C_{port} is greater than or equal to 180μF so that I_{Inrush} max is satisfied.	M	Yes [ ]
PD20	Peak operating current.	33.3.5.4	Not to exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max.	M	Yes [ ]
PD21	Peak current.	33.3.5.4	Not to exceed I_{Port} max.	M	Yes [ ]
PD22	RMS, DC, and ripple current.	33.3.5.4	Bounded by $Irms = [(Idc)^2 + (Iac)^2]^{1/2}$.	M	Yes [ ]
PD23	Maximum operating DC and RMS current.	33.3.5.4	Defined by the following equation: I_{Port_max} [mA] =12950/ V_{Port}.	M	Yes [ ]
PD24	PI capacitance during normal powering mode.	33.3.5.5	As specified in subclause 33.3.5.5.	M	Yes [ ]
PD25	Ripple and noise.	33.3.5.6	As specified in Table 33–12 for the common-mode and/or differential pair-to-pair noise at the PD PI.	M	Yes [ ]
PD26	Ripple and noise specification.	33.3.5.6	For all operating voltages in the range defined by Table 33–12 item 1.	M	Yes [ ]
PD27	Ripple and noise presence.	33.3.5.6	Must operate correctly when connected to a PSE generating ripple and noise levels specified in Table 33–5 item 3.	M	Yes [ ]
PD28	Power supply turn on/turn off voltages.	33.3.5.7	As specified in Table 33–12 when connected to a PSE through a 20Ω series resistor.	M	Yes [ ]
PD29	Startup oscillations	33.3.5.7	Shall turn on or off without startup oscillations and within the first trial at any load value.	M	Yes [ ]
PD30	Classification stability.	33.3.5.8	Classification signature will remain valid within T_{class} and remain valid for the duration of the classification period.	M	Yes [ ]
PD31	Backfeed voltage	33.3.5.10	Mode A and Mode B per 33.3.5.10.	M	Yes [ ]
PD32	Maintain power signature.	33.3.6	(current draw) and (AC impedance) defined in Table 33–13.	M	Yes [ ]
PD33	No longer require power.	33.3.6	Remove both components of the Maintain Power Signature.	M	Yes [ ]

33.7.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Electrical isolation	33.4.1	Electrical isolation will be in accordance with subclause 6.2 of IEC 60950-1:2001	M	Yes [ ]
EL2	Strength tests for electrical isolation.	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1.	M	Yes [ ]
EL3	Isolation and grounding requirements.	33.4.1	Conductive link segments that have different requirements must have those requirements provided by the port-to-port isolation of the NID.	M	Yes [ ]
EL4	Environment A requirements for multiple instances of PSE and/or PD.	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	!MID:M	Yes [ ] N/A [ ]
EL5	Environment A requirement.	33.4.1.1.1	Switch more negative conductor.	M	Yes [ ]
EL6	Environment B requirements for multiple instances of PSE and/or PD.	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated.	M	Yes [ ]
EL7	Fault tolerance for PSEs and PDs encompassed within the MDI.	33.4.2	Meet requirements of the appropriate specifying clause.	!MID:M	Yes [ ] N/A [ ]
EL8	Fault tolerance for PSEs and PDs not encompassed within an MDI.	33.4.2	Meet the requirements of 33.4.2.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL9	Common-mode fault tolerance.	33.4.2	Each wire pair will withstand a 1000V common-mode impulse applied at Ecm of either polarity without damage.	M	Yes [ ]
EL10	The shape of the impulse for item common-mode fault tolerance.	33.4.2	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of the half value).	M	Yes [ ]
EL11	Impedance balance for transmit and receive pairs.	33.4.3	Exceed: - 29-17 log 10 (f/10)dB from 1.0 to 20MHz for 10Mb/s PHYs - 34-19.2 log 10 (f/50)dB from 1.0 to 100MHz for 100Mbits/s or greater PHYs.	M	Yes [ ]
EL12	Common-mode output voltage.	33.4.4	Magnitude while transmitting data and with power applied will not exceed 50mV peak when operating at 10Mbits/s and 50mV peak-to-peak when operating at 100Mbits/s or greater.	M	Yes [ ]
EL13	Common-mode AC voltage.	33.4.4	Magnitude at all other ports will not exceed 50mV peak-to-peak.	M	Yes [ ]
EL14	Frequency range for common-mode AC voltage measurement.	33.4.4	At all other ports will be from 1MHz to 100MHz.	M	Yes [ ]
EL15	Common-mode output voltage test configuration.	33.4.4	Must be performed with the PHY transmitting data and an operating PSE or PD and with the PSE load or PD source requirements specified in 33.4.4 items 1) or 2).	M	Yes [ ]
EL16	Noise from an operating PSE or PD to the differential transmit and receive pairs.	33.4.6	Will not exceed 10mV peak-to-peak measured from 1MHz to 100MHz.	M	Yes [ ]
EL17	Differential noise voltage test setup.	33.4.6	The PSE and PD shall be terminated as illustrated in Figure 33–16 and tested with the PSE and PD conditions as specified in 33.4.4.	M	Yes [ ]
EL18	Return loss requirements.	33.4.7	Specified in 14.3.1.3.4 for a 10Mb/s PHY, in ANSI X3.263:1995 for a 100Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY.	M	Yes [ ]

33.7.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	PSE electrical isolation.	33.4.1	Provided between port device circuits, frame ground and PI leads.	M	Yes [ ]
PSEEL2	Short circuit fault tolerance.	33.4.2	Any wire pair will withstand any short circuit to any other pair for an indefinite amount of time.	M	Yes [ ]
PSEEL3	Magnitude of short circuit current.	33.4.2	Not to exceed maximum value of I_{LIM}.	M	Yes [ ]
PSEEL4	Limitation of electromagnetic interference.	33.4.5	PSE will comply with applicable local and national codes.	M	Yes [ ]
PSEEL5	Insertion of Midspan at FD.	33.4.8	Comply with the guidelines specified in 33.4.8 items a) and b).	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”.	33.4.8	Installation of a Midspan PSE will not increase the length to more than 100 meters as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE.	33.4.8	Must not alter transmission requirements of the “permanent link”.	MID:M	Yes [ ] N/A [ ]
PSEEL8	Midspan PSE insertion in the channel.	33.4.8	Must provide continuity for signal pairs.	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan continuity in non-data pairs.	33.4.8	Will not provide DC continuity between the two sides of the segment for the pairs that inject power.	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE inserted as a “Connector” or “Telecom outlet.”	33.4.8.1	Meet transmission parameters NEXT, insertion loss and return loss.	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT.	33.4.8.1.1	$NEXT_{conn} \geq 40 - 20\log(f/100)$dB (equation 33–5) but not greater than 65dB from from 1MHz to 100MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Insertion Loss.	33.4.8.1.2	$Insertion\_loss_{conn} \leq 0.04$ SQRT(f) dB [Equation (33–6)] but not less than 0.1dB from from 1MHz to 100MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL13	Midspan PSE Return Loss.	33.4.8.1.3	$1MHz \leq f < 20MHz$: 23dB $20MHz \leq f \leq 100MHz$: 14 dB (Table 33–14) for transmit and receive pairs.	MID:M	Yes [ ] N/A [ ]
PSEEL14	Work area or equipment cable Midspan PSE.	33.4.8.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 for insertion loss, NEXT, and return loss for all transmit and receive pairs.	MID:M	Yes [ ] N/A [ ]

33.7.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD electrical isolation.	33.4.1	Provided between all external conductors, including frame ground, and all PI leads.	M	Yes [ ]
PDEL2	PD common-mode test requirement.	33.4.4	The PIs that require power shall be terminated as illustrated in Figure 33–16.	M	Yes [ ]

33.7.3.7 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety.	33.5.1	Conform to IEC publication 60950-1:2001.	M	Yes [ ]
ES2	Safety.	33.5.1	Comply with all applicable local and national codes.	M	Yes [ ]
ES3	Telephony voltages.	33.5.6	Application thereof described in 33.5.6 not result in any safety hazard.	M	Yes [ ]
ES4	Limitation of electromagnetic interference.	33.5.7	Comply with applicable local and national codes.	M	Yes [ ]

33.7.3.8 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety.	33.5.1	Limited Power Source in accordance with IEC publication 60950-1:2001.	M	Yes [ ]
PSEES2	Resistance unbalance.	33.5.5	As specified in IEC 11801 Edition 2 Clause 6.4.8 (reference: 3 percent).	M	Yes [ ]

33.7.3.9 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability.	33.6	Access via MII, GMII, or equivalent.	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers.	33.6.1	Register address 11 for control functions and register address 12 for status functions.	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH).	33.6.1	Remain high until read via the management interface.	MAN:M	Yes [ ] N/A [ ]
MF4	Register bits read.	33.6.1	Bit assumes a value based on the current state of the condition it monitors.	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:4).	33.6.1.1.1	Not affected by writes and return a value of zero when read.	MAN:M	Yes [ ] N/A [ ]
MF6	Pair Control Ability not supported.	33.6.1.1.2	Ignore writes to bits 11.3:2.	MAN∗ !PCA:M	Yes [ ] N/A [ ]
MF7	Writes to 11.3:2 when Pair Control Ability not supported.	33.6.1.1.2	Return the value that reports the supported PSE Pinout Alternative.	MAN∗ !PCA:M	Yes [ ] N/A [ ]
MF8	Bits 11.3:2 set to '01'.	33.6.1.1.2	Forces the PSE to use Alternative A.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF9	Bits 11.3:2 set to '10'.	33.6.1.1.2	Forces the PSE to use Alternative B.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF10	Pair control ability bit, (12.0).	33.6.1.1.2	A value of ‘1’ sets the mr_pse_alternative variable.	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF11	PSE function disabled	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘00’, also the MDI shall function as it would if it had no PSE function.	MAN:M	Yes [ ] N/A [ ]
MF12	PSE function enabled.	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘01’.	MAN:M	Yes [ ] N/A [ ]
MF13	PSE enable bits (11.1:0).	33.6.1.1.3	Writing to these register bits shall set mr_pse_enable to the corresponding value: 00 = disable, 01 = enable and 10 = force power.	MAN:M	Yes [ ] N/A [ ]
MF14	Reserved bits (12.15:13).	33.6.1.2.1	Not affected by writes and shall return a value of zero when read.	MAN:M	Yes [ ] N/A [ ]
MF15	Power denied bit (12.12).	33.6.1.2.2	A value of ‘1’ indicates power has been denied.	MAN:M	Yes [ ] N/A [ ]
MF16	Power denied bit implementation.	33.6.1.2.2	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF17	Valid signature bit (12.11).	33.6.1.2.3	Logic ‘1’ indicates a valid signature has been detected.	MAN:M	Yes [ ] N/A [ ]
MF18	Valid signature bit implementation.	33.6.1.2.3	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF19	Invalid signature bit (12.10).	33.6.1.2.4	Logic ‘1’ indicates an invalid signature has been detected.	MAN:M	Yes [ ] N/A [ ]
MF20	Invalid signature bit implementation.	33.6.1.2.4	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF21	Short circuit bit (12.9).	33.6.1.2.5	Logic ‘1’ indicates a short circuit condition has been detected.	MAN:M	Yes [ ] N/A [ ]
MF22	Short circuit bit implementation.	33.6.1.2.5	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF23	Overload bit (12.8).	33.6.1.2.6	Set to ‘1’ when PSE state diagram enters the state ‘ERROR_DELAY_OVER’.	MAN:M	Yes [ ] N/A [ ]
MF24	Overload bit implementation.	33.6.1.2.6	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]
MF25	MPS absent bit (12.7).	33.6.1.2.7	Read as logic 1 indicates either or both elements of the MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.10.	MAN:M	Yes [ ] N/A [ ]
MF26	MPS Absent bit implementation.	33.6.1.2.7	Will be implemented with a latching high behavior as defined in 33.6.1.	MAN:M	Yes [ ] N/A [ ]